Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claims 1-22. Please add new claims 23-40.

23. (new): A system core comprising:

a processor;

a direct memory access (DMA) controller;

an instruction memory containing processor instructions and DMA instructions;

a plurality of memories, the DMA controller coupled to the instruction memory and the plurality of memories, the DMA controller fetching and executing DMA instructions from the instruction memory to populate the plurality of memories with data from an external device, the processor operating on the data found in the populated memories.

24. (new): The system core of claim 23 wherein the executed DMA instructions specify a pattern to populate the plurality of memories.

25. (new): The system core of claim 24 wherein the pattern is a block, circular, or stride pattern.

26. (new): The system core of claim 23 wherein the data from the external device includes processor instructions.

27. (new): The system core of claim 23 further comprising:

a DMA bus connecting the DMA controller to the instruction memory and the plurality of memories.

28. (new): The system core of claim 23 further comprising:

a bus coupled to the external device and the system core.

29. (new): The system core of claim 23 wherein the external device is an external host processor.

30. (new): The system core of claim 23 wherein the external device is an external synchronous data random access memory (SDRAM).

31. (new): The system core of claim 23 wherein the DMA controller fetches and executes DMA instructions from the instruction memory to populate the external device with data from the plurality of memories.

32. (new): A method for transferring data between a system core and an external device, the system core having instruction memory and a plurality of memories, the method comprising:

fetching direct memory access (DMA) instructions from instruction memory;

executing the fetched DMA instructions to populate the plurality of memories with data from the external device; and

transferring data from the external device to the plurality of memories.

33. (new): The method of claim 31 wherein the executed DMA instructions specify a pattern to populate the plurality of memories.

34. (new): The method of claim 32 wherein the pattern is a block, circular, or stride pattern.

35. (new): The method of claim 31 wherein the data from the external device includes processor instructions.

36. (new): The method of claim 31 wherein the external device is an external host processor.

37. (new): The method of claim 31 wherein the external device is an external synchronous data random access memory (SDRAM).

38. (new): The method of claim 31 further comprising:

executing the fetched DMA instructions to populate the external device with data from the plurality of memories; and

transferring data the plurality of memories to from the external device.

39. (new): The method of claim 38 wherein both transferring steps occur simultaneously.

40. (new): The method of claim 32 wherein the system core contains a sequential processor (SP) which executes the data transferred from the external device as instructions.